AS5203 Ultra Low Jitter Low Power I²C Programmable Differential DCTCXO

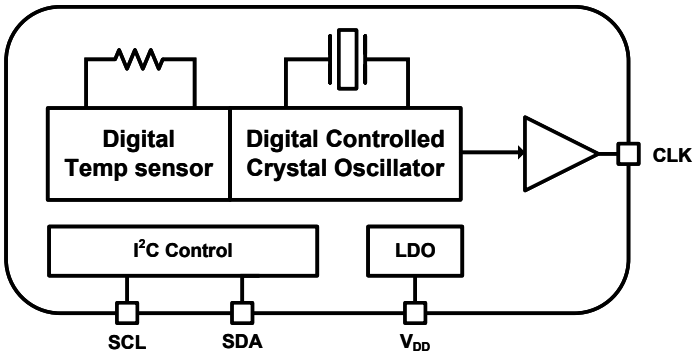
Description

The AS5203 is a digitally controlled temperature compensated crystal oscillator (DCTCXO) with a pair of differential output clocks between 10 MHz and 156.25 MHz. The AS5203 utilizes digital temperature sensing and frequency compensation technologies to provide a high precision, temperature stabilized clock with grade options from ±5ppm to ±20ppm.

The AS5203 operates in a wide power supply range from 1.8V to 3.3V. The on-chip LDOs ensure robust power supply noise rejection which simplifies the external supply noise filtering requirements.

The AS5203 supports in-system programmability after powered up at a default output driver format and clock output frequency. The device supports programmable universal clock driver formats including LVDS, LVPECL, HCSL, CMOS etc. Its digitally controlled oscillator (DCO) mode supports glitchless frequency pulling range up to ±25ppm.

Available in industry standard 2520, 3225, 5032 packages, the AS5203 comes in industrial, extended industrial and automotive device grades. Specific combination of package, stability, default frequency, default driver format, I2C address and device grade can be selected at the time of ordering.



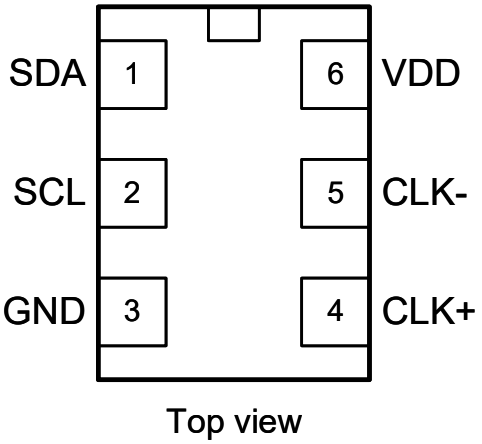
Key Features

- Frequency range: 10 to 156.25 MHz
- LVPECL, LVDS, CML, HCSL, CMOS, or Dual CMOS output options
- Ultra-low jitter: 52 fs Typ
  (12 kHz – 20 MHz, @156.25 MHz)
- Ultla-low core power: 5mA
- Operating temperature range:
  - -40 to 85 ℃ (Industial grade)
  - -40 to 105 ℃ (Extended-Industial grade)
  - -40 to 105 ℃ (AEC-Q100 grade 2)
- Temperature stability:
  - ±5 ppm (Grade S)
  - ±20 ppm (Grade D)
- Programmable output frequencies and formats by I²C communication interface
- Integrated LDO for on-chip power supply noise filtering
- 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Standard DFN 2520, 3225 and 5032 packages

Application

- Microwave backhaul
- Communication networks
- Data center interconnect
- AI server clusters
- Smart network interface card
- High-speed optical module

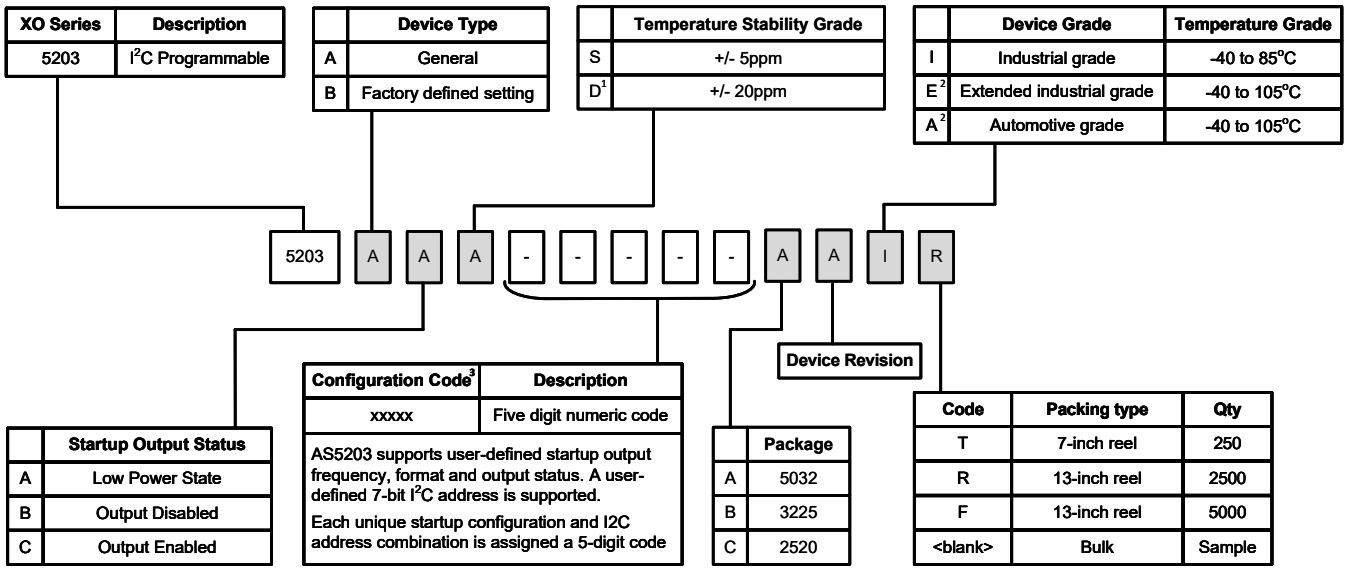
Pin definition



Top view

Pin#	Description
1	SDA = I²C serial data
2	SCL = I²C serial clock
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output
6	VDD = Power supply

1. Ordering Guide



Note:

1. Temperature compensation is not applied for grade-D device. Frequency is calibrated at 25 ℃ in production test.
2. Contact Aeonsemi for “Extended industrial” and “Automotive” grade device.
3. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	—	85	℃	Industrial grade
		-40	—	105	℃	Extended industrial grade
		-40	—	105	℃	Automotive AEC-Q100 Grade2
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.71	—	3.63	V	Core voltage
Supply Current (F_{CLK} = 156.25 MHz)	I_{CORE}	—	4	5	mA	Tristate Hi-Z (Output disabled)
	I_{DRV}	—	31	33	mA	LVPECL (Standard)
		—	18	20	mA	LVPECL (Self-Biased)
		—	8	10	mA	LVDS
		—	18	20	mA	HCSL
		—	18	20	mA	CML
		—	6	8	mA	1.8V LVCMOS (C_L = 15 pF)
		—	8	10	mA	2.5V LVCMOS (C_L = 15 pF)
		—	10	13	mA	3.3V LVCMOS (C_L = 15 pF)
Frequency Range						
Frequency Range	F_{CLK}	10	—	156.25	MHz	Standard frequency options
		10, 16, 19.2, 20, 25, 26, 32, 38.4, 50, 52, 100, 155.52, 156.25				Contact Aeonsemi for other frequency options
Frequency Tolerance						
Initial frequency accuracy[1]	F_{INIT}	-2	—	2	ppm	Grade S
		-5	—	5	ppm	Grade D
Temperature stability over full temp range[2]	F_{STAB}	-5	—	5	ppm	Grade S
		-20	—	20	ppm	Grade D
Aging	S_{AGING}	-1	—	1	ppm/y	Maximum aging slope at 25 ℃
	F_{AGING}	-3	—	3	ppm	10-year aging at 25℃
Notes: 1. Inclusive of initial frequency tolerance at 25℃, variations over supply voltage, load and humidity after 2 times of reflows. 2. Frequency / temperature characteristics with offset removed.						
IO Characteristics						
SDA, SCL	V_{IH}	0.7×V_{DD}	—	—	V	Input high voltage
	V_{IL}	—	—	0.3×V_{DD}	V	Input low voltage
	V_{OH}	0.83×V_{DD}	—	—	V	Output high voltage
	V_{OL}	—	—	0.17×V_{DD}	V	Output low voltage

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Characteristics						
Powerup time	T_{OSC}	—	—	4	ms	Time from power reaches 0.9 × V_{DD} to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	—	55	%	All formats
Rise/Fall time (20% to 80% VPP)	$T_{R/F}$	—	0.5	1.5	ns	LVCMOS (C_L = 15 pF)
		—	—	350	ps	LVPECL / LVDS / CML
		—	—	550	ps	HCSL
LVPECL (Standard)	V_{OC}	V_{DD}-1.55	V_{DD}-1.4	V_{DD}-1.25	V	Mid-level
	V_O	1.35	1.6	1.85	V_{PP}	Swing (Diff)
LVPECL (Self-Biased)	V_O	1.35	1.6	1.85	V_{PP}	Swing (Diff)
LVDS	V_{OC}	1.125	1.20	1.275	V	Mid-level (2.5V, 3.3V V_{DD})
		0.78	0.85	0.92	V	Mid-level (1.8V V_{DD})
	V_O	0.64	0.8	0.96	V_{PP}	Swing (Diff)
HCSL (R_{TERM} = 50 Ω)	V_{OC}	0.35	0.4	0.45	V	Mid-level
	V_O	1.28	1.6	1.92	V_{PP}	Swing (Diff)
HCSL (R_{TERM} = 42.5 Ω)	V_{OC}	0.35	0.4	0.45	V	Mid-level
	V_O	1.29	1.62	1.94	V_{PP}	Swing (Diff)
CML	V_{OC}	V_{DD}-0.35	V_{DD}-0.4	V_{DD}-0.45	V	Mid-level
	V_O	1.28	1.6	1.92	V_{PP}	Swing (Diff)
LVCMOS	V_{OH}	0.83×V_{DD}	—	—	V	C_L = 15 pF
	V_{OL}	—	—	0.17×V_{DD}	V	
Phase Noise and Jitter						
RMS jitter BW: 12k - 20MHz	R_J	—	52	70	fs	F_{CLK} >= 100 MHz
		—	100	200	fs	F_{CLK} >= 50 MHz
		—	150	300	fs	F_{CLK} <50 MHz
Phase noise 156.25MHz LVDS output V_{DD} = 1.8 - 3.3V	PN_{1k}	—	-137	—	dBc/Hz	Phase noise at 1kHz offset
	PN_{10k}	—	-148	—	dBc/Hz	Phase noise at 10kHz offset
	PN_{100k}	—	-155	—	dBc/Hz	Phase noise at 100kHz offset
	PN_{1M}	—	-162	—	dBc/Hz	Phase noise at 1MHz offset
	PN_{10M}	—	-163	—	dBc/Hz	Phase noise at 10MHz offset
PSNR						
Spurs from power noise 50mV ripple V_{DD} = 1.8V	PSNR	—	-76	—	dBc	100 kHz sine wave
		—	-75	—	dBc	200 kHz sine wave
		—	-75	—	dBc	500 kHz sine wave
		—	-75	—	dBc	1 MHz sine wave
Spurs from power noise 50mV ripple V_{DD} = 2.5 or 3.3V	PSNR	—	-83	—	dBc	100 kHz sine wave
		—	-83	—	dBc	200 kHz sine wave
		—	-83	—	dBc	500 kHz sine wave
		—	-82	—	dBc	1 MHz sine wave

Table 2.2. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	3

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.3. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	℃
Storage temperature	T_S	-55 - 125	℃
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	℃
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

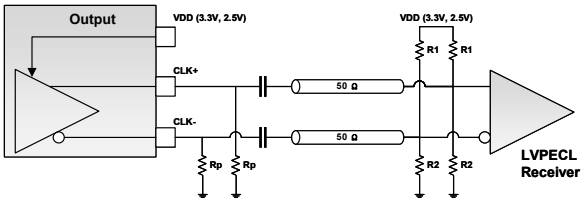
Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

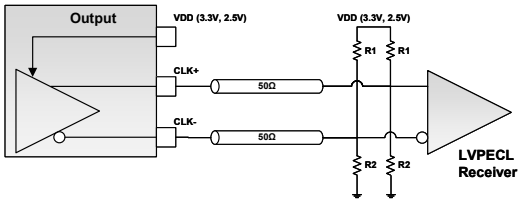
3. Recommended Output Terminations

3.1. Differential Output

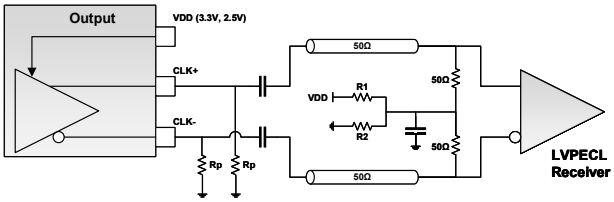
The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.



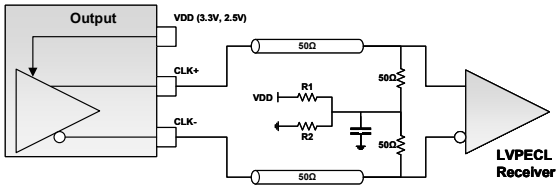
AC-Coupled LVPECL - Thevenin Termination



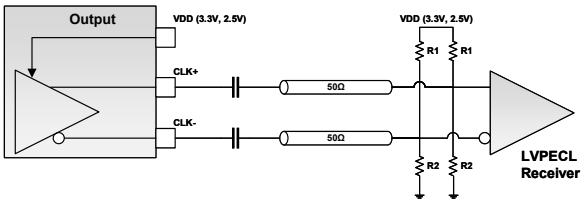
DC-Coupled LVPECL - Thevenin Termination



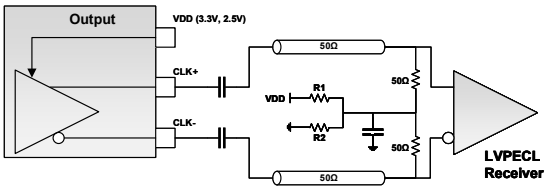
AC-Coupled LVPECL - 50 Ω with VTT Bias



DC-Coupled LVPECL - 50 Ω with VTT Bias



AC-Coupled Self-Biased LVEPCL - Thevenin Termination



AC-Coupled Self-Biased LVEPCL - 50 Ω with VTT Bias

Figure 3.1. LVPECL Output Terminations

Table 3.1. LVPECL Termination Resistor Values

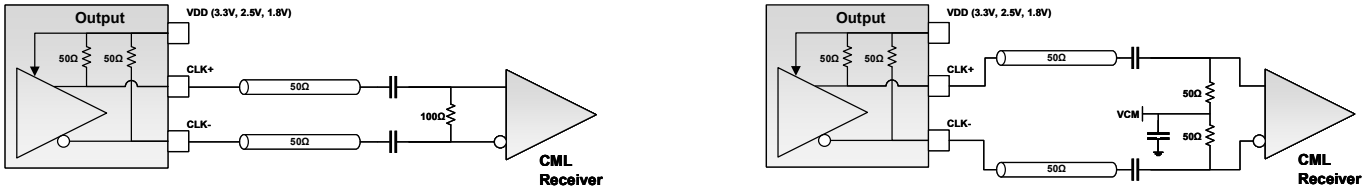
AC Coupled LVPECL Termination Resistor Values			
V_{DD}(V)	R_P	R_1	R_P
3.3 V	158 Ω	127 Ω	82.5 Ω
2.5 V	92 Ω	250 Ω	62.5 Ω

DC Coupled LVPECL Termination Resistor Values		
V_{DD}(V)	R_1	R_2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω

AC-Coupled LVDS

DC-Coupled LVDS

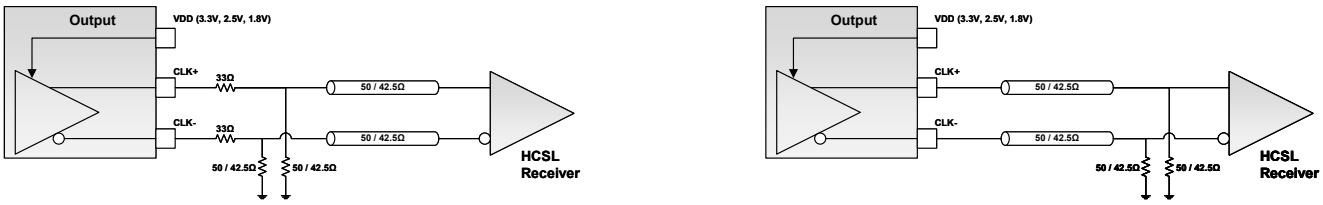
Figure 3.2. LVDS Output Terminations



AC-Coupled CML without VCM

AC-Coupled CML with VCM

Figure 3.3. CML Output Terminations



Source Terminated HCSL

Destination Terminated HCSL

Figure 3.4. HCSL Output Terminations

3.2. CMOS Output

Dual CMOS output format options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single AS5203 device.

Figure 3.5. Integrated 1:2 CMOS Buffer Supports In-Phase or Complementary Outputs

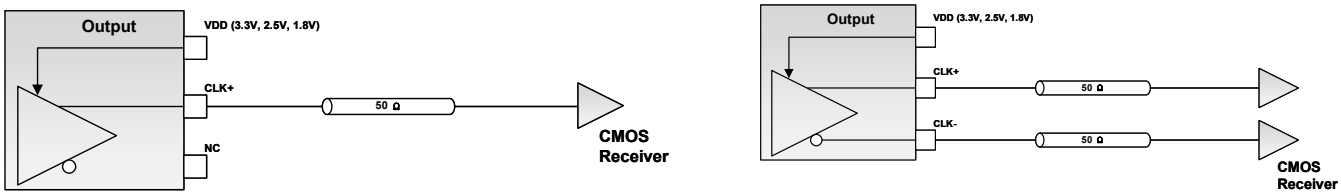


Figure 3.6. LVCMOS Output Terminations

4. Configuring via I²C Interface

4.1. I²C Serial Interface

The I²C interface on the AS5203 is fully compatible with the "UM10204 I2C-bus specification and user manual, Rev. 6 - 4 April 2014" standard, as described in Table 4.1.

Table 4.1. I²C Compatibility

I²C Protocol	Speed	Compliance	Notes
Standard	100 kHz	Compliant	N/A
Fast	400 kHz	Compatible	SDA failing edge can be faster than 20 ns depending on loading.
Fast+	1 MHz	Compatible	SDA falling edge can be faster than 20 ns depending on loading. SDA max pull down current is 6 mA.

4.2. I²C Register Write and Read Protocol

AS5203 implements an 8-bit I²C address space with 256 addressable byte register locations. Certain device register and bits are reserved, and they must not be changed from their default reset state. In an I²C bus system, the AS5203 acts as a slave device connected to the I²C serial interface bus. It is accessed via a 7-bit factory programmed (per user specification) slave address. Allowed values of this device address are in the range from 8 to 119. Both write and read register transactions with register address auto increment are enabled as shown in Figure 4.1.

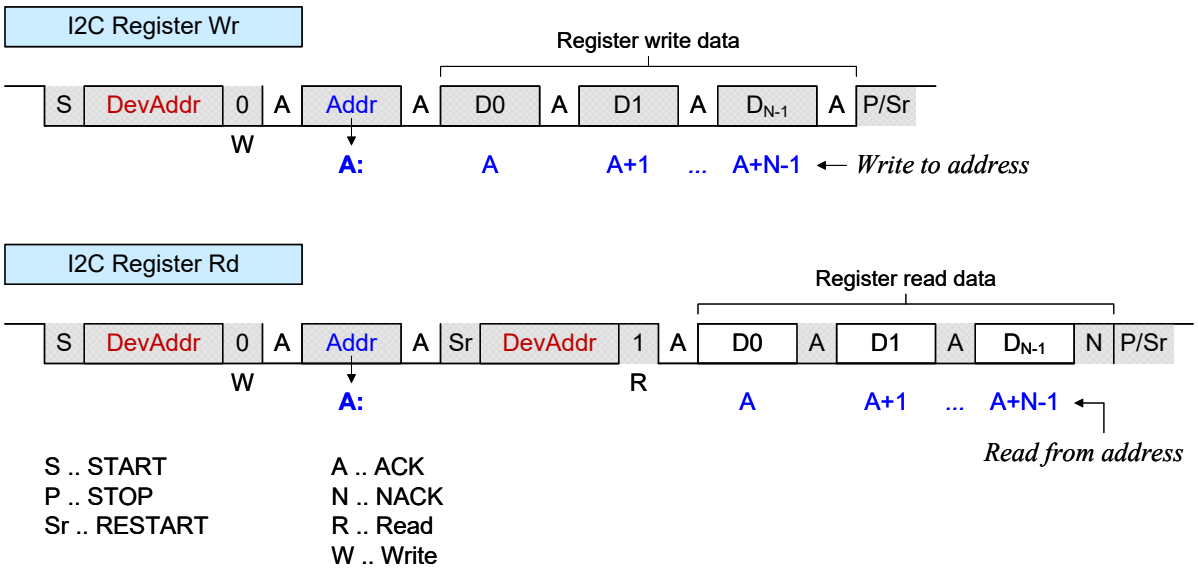


Figure 4.1. I²C Write and Read Transactions

Write register transaction is an I²C write transaction with an 8-bit register address data byte stream. It is followed by one or more register data bytes. Read register sequence starts after a write transaction to set the read register address. It is followed by the I²C read transaction to read one or more data bytes.

The register address autoincrement is enabled upon power up. It is incremented till a maximum address 0xFF of the I²C register space is reached.

Data and address bytes appear on the SDA bus with the most significant bit (MSB) first per I²C standard. During I²C transactions, SCL clock bus is never stalled by the device.

4.3. I²C Register Reference

The I²C interface is a byte-oriented interface. Registers are wider than 8 bits requiring to be split into multiple bytes located on subsequent register addresses. There are two types of multi byte registers:

1. Array of arrays, prefix ab, for example abUSER_ID[4] are organized in little endian fashion, byte abUSER_ID[0] is located at the lowest address, and the last byte of the array abUSER_ID[3] is located at the highest address.
2. An assigned 32-bit long integer, prefix j, and a 32-bit IEEE 754-2008 floating point number, prefix f are organized in big endian fashion, such that the most significant byte (MSB) is located at the lowest address.

Any unassigned byte registers have prefix b. Registers in the I²C address space 0x00...0xFF without specifications in the register description table are reserved for factory use. All register bit fields labeled [reserved] are read only and are reserved for factory use. Read value should be ignored. Any register bits not specifically mentioned in “Bits” columns are unused. Writing to these registers is ignored and a read always returns a 0. Numerical values are either hexadecimal with 0x prefix or decimal without any prefix.

Descriptions of register table columns:

Table 4.2. Register Table Columns

Register	Description
Addr	I²C register address.
Register	Register name.
Bytes	Number of bytes in the register. Wider than single byte registers span several subsequent bytes in an address space.
Endian	Endian for registers wider than one byte. Not applicable for single byte registers.
B	Big endian. The most significant byte (MSB) of the register appears at the lowest address.
L	Little endian. The least significant byte (LSB) of the register appears at the lowest address.
Field	Field name within the register.
[reserved]	Reserved for factory use and readable only
Bits	Field bit locations within a register. When the field spans more than one bit, the [M:L] notate. Denoting locations of a most significant bit M and a least significant bit L within the register are used.
Type	Field access type.
R/W	Read/write field by I²C.
R	Read only field by I²C.
W1	Writing a 1 triggers an associated event, while writing a 0 has no effect. A read always returns 0.
Rst	Field reset value. The value ‘Factory’ indicates that the value depends on the individual device factory configuration.

4.4. Register Map

The device incorporates a Digital Controlled Oscillator (DCXO) feature to allow seamless and fast setting of the frequency deviation from the center frequency. Table 4.3. shows the DCXO configuration registers.

Table 4.3. DCXO Configuration Registers

Register	Addr	Field	Bits	Type	Rst	Description
dcxo_wdata[4]	0x8b	wdata	[31:0]	R/W	0	Frequency offset to write to DCXO in signed 32-bit, big endian format.
dcxo_step[4]	0x8f	step	[31:0]	R/W	0	Frequency step to write to DCXO in signed 32-bit, big endian format.
dcxo_ctrl	0x93	step_dir	[2]	R/W	0	Controls the step is applied positively or negatively: 0: Down 1: Up
		step_apply	[1]	W1	0	Adds extra offset to the DCXO by the amount of step
		clr	[0]	W1	0	Synchronously resets the DCXO DSP.
dcxo_rdata[4]	0x95	rdata	[31:0]	R	0	DCXO data register through which the actual DCXO control data is applied. The data is in signed 32-bit, big endian format. The added frequency per LSB depends on the device's frequency and crystal used.

5. Package Outline Drawing

Figure 5.1. shows the package outline drawing for the AS5203 devices. Details of dimension for different size options are listed in Table 5.1.

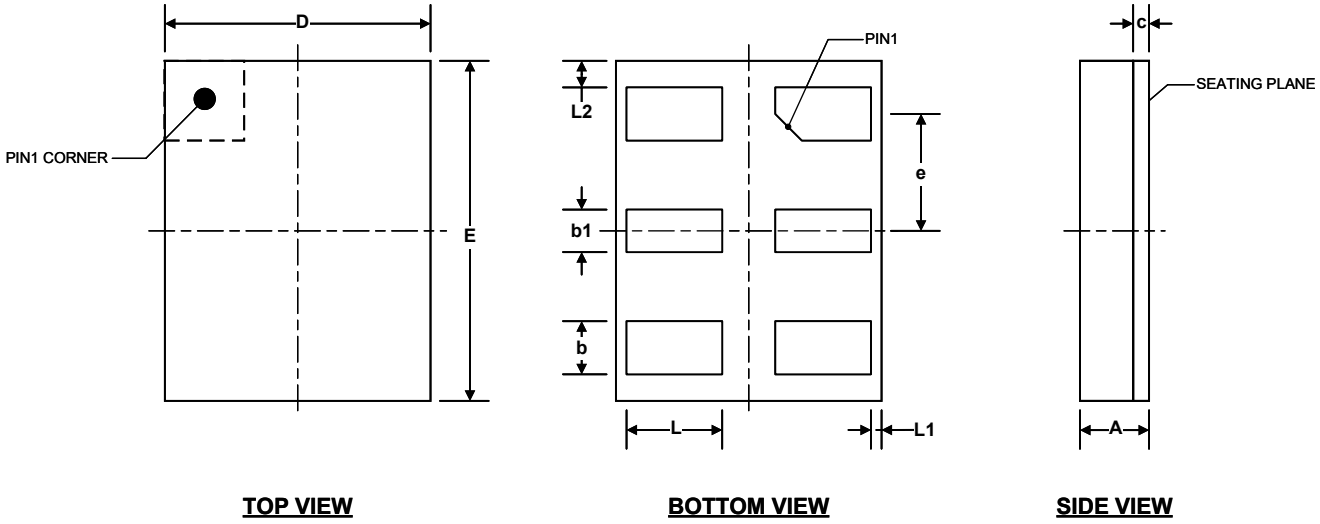


Figure 5.1. Package Outline Drawing

Table 5.1. Dimensions of Package Outline Drawing (mm)

Symbol	5032 Package	3225 Package	2520 Package
A	1.146 ± 0.100	1.146 ± 0.100	0.876 ± 0.100
b	0.640 ± 0.050	0.600 ± 0.050	0.380 ± 0.050
b1	0.640 ± 0.050	0.600 ± 0.050	0.380 ± 0.050
D	3.200 ± 0.100	2.500 ± 0.050	2.000 ± 0.050
e	1.270 BSC	1.100 BSC	0.900 BSC
E	5.000 ± 0.100	3.200 ± 0.050	2.500 ± 0.050
L	0.900 ± 0.075	0.700 ± 0.075	0.550 ± 0.075
L1	0.100 ± 0.075	0.100 ± 0.075	0.100 ± 0.075
L2	0.910 ± 0.075	0.200 ± 0.075	0.160 ± 0.075

6. Recommended PCB Land Pattern

Figure 6.1. shows the drawing of recommended PCB land pattern for the AS5203 devices. Details of dimension for different size options are listed in Table 6.1.

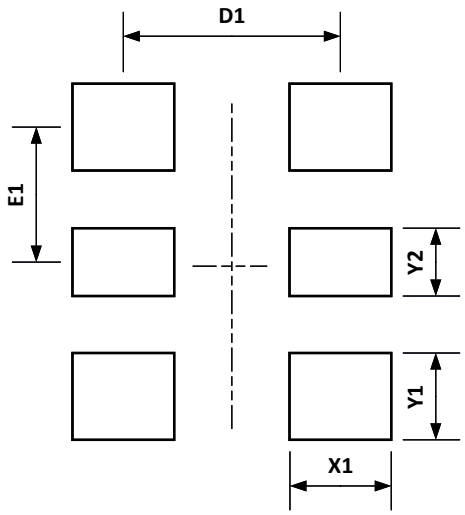


Figure 6.1. Recommended PCB Land Pattern

Table 6.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	5032 Package	3225 Package	2520 Package
D1	2.20	1.70	1.35
E1	1.27	1.10	0.90
X1	1.20	1.00	0.85
Y1	0.84	0.80	0.58
Y2	0.84	0.80	0.58

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Mark

Figure 7.1. shows the top mark specifications for the AS5203 devices. Description of each line is listed in Table 7.1.

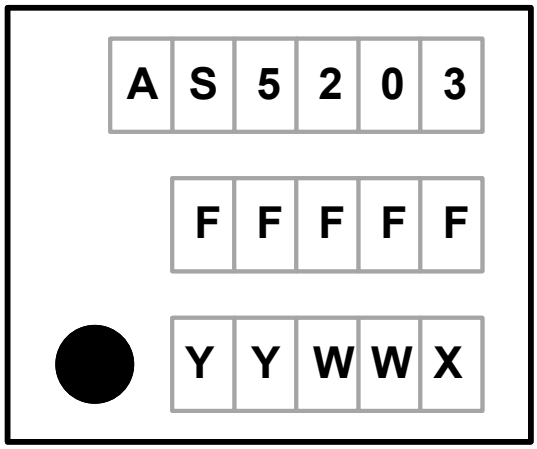


Figure 7.1. Top Mark

Table 7.1. Top Mark Description

Line	Position	Description
1	1-6	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

8. Important Notice and Disclaimer

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9. Revision History

Revision	Date	Description
1.02	Sep 2025	Corrected several description errors
1.01	Aug 2025	Officially release as mass production version
0.09	Feb 2025	Added frequency options; “2520” package outline diagram
0.08	Aug 2024	Added “5032” & “3225” package outline diagram
0.07	Apr 2024	Added “2520” package option
0.06	Feb 2024	Updated the “Ordering guide”
0.05	Aug 2023	Revised the stability for D-grade option
0.04	Jul 2023	Updated the package outline
0.03	Jun 2023	Updated the “Ordering guide” and added phase noise jitter for clock >=100 MHz
0.02	Feb 2023	Updated the “Temperature Stability Grade” D grade
0.01	Nov 2021	Preliminary release