

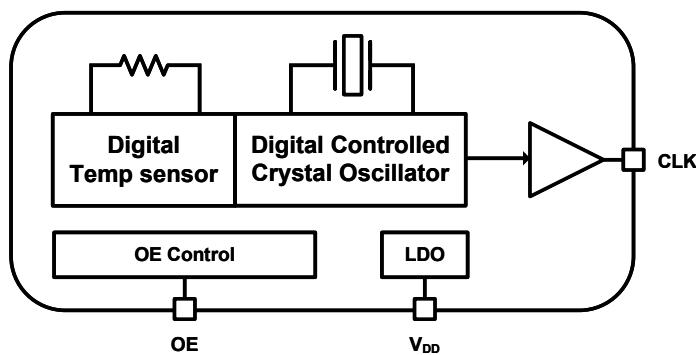
AS5231 Ultra Low Jitter Low Power LVC MOS TCXO

Description

The AS5231 is a temperature compensated crystal oscillator (TCXO) with a low-amplitude LVC MOS output clock between 10 MHz and 76.8 MHz. The AS5231 utilizes digital temperature sensor and frequency compensation technologies to provide a high precision, temperature stabilized clock with grade options from $\pm 0.5\text{ppm}$ to $\pm 20\text{ppm}$.

The AS5231 operates in a wide power supply range from 1.5V to 3.3V. The on-chip LDOs provides robust power supply noise rejection which simplifies the external supply noise filtering requirements. The AS5231 supports configurable output amplitude from 0.8V to 1.2V. The 0.8V output option is compliant with clipped sine (0.8V CS) which is widely adopted in the industry.

Available in industry-standard 2016 package, the AS5231 comes in industrial, extended industrial and automotive device grades. Specific combination of package, frequency, stability, driver format, and device grade can be selected at the time of ordering.



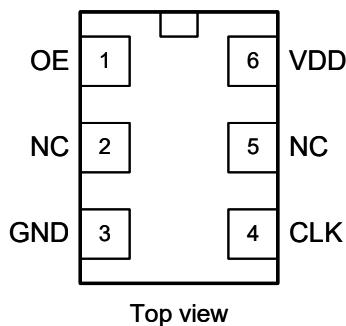
Key Features

- Frequency range: 10 to 76.8 MHz
- 0.8, 1.0, 1.2V LVC MOS output options
- Ultra-low jitter: 93 fs Typ RMS (12 kHz – 20 MHz, @76.8 MHz)
- Operating temperature range:
 - -40 to 85 °C (Industrial grade)
 - -40 to 105 °C (Extended-Industrial grade)
 - -40 to 105 °C (AEC-Q100 grade 2)
- Temperature stability:
 - $\pm 0.5\text{ ppm}$ (Grade C)
 - $\pm 20\text{ ppm}$ (Grade D)
- Integrated LDO for on-chip power supply noise filtering
- 1.5V to 3.3V V_{DD} supply operation
- Standard DFN 2016 package

Application

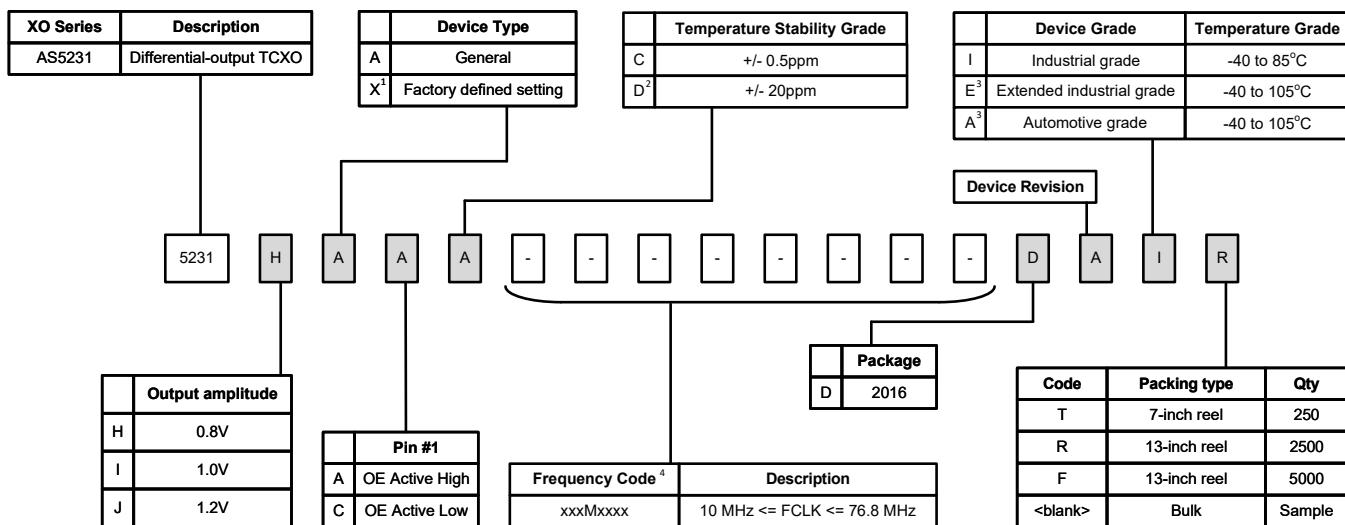
- Precision GNSS systems
- Microwave backhaul
- Narrow-band communications
- Storage and servers
- Test and measurements

Pin definition



Pin#	Description
1	OE = Output enable. Active high
2	NC = Not connect
3	GND = Ground
4	NC = Not connect
5	CLK = Clock output
6	VDD = Power supply

1. Ordering Guide



Note:

1. "X" refers to the ID for the unique configuration with factory-defined settings, the value ranges from "B" to "Z".
2. Temperature compensation is not applied for grade-D device. Frequency is calibrated at 25 °C in production test.
3. Contact Aeonsemi for "Extended industrial" and "Automotive" grade device.
4. For example: 38.4 MHz = 38M40000; 76.8 MHz = 76M80000.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T _A	-40	—	85	°C	Industrial grade
		-40	—	105	°C	Extended industrial grade
		-40	—	105	°C	Automotive AEC-Q100 Grade2
Supply Voltage and Power Consumption						
Supply Voltage	V _{DD}	1.71	—	3.63	V	Core voltage
Driver Regulator Voltage	V _R	0.8	—	1.2	V	Regulator voltage
Supply Current (F _{CLK} = 38.4 MHz)	I _{CORE}	—	4	5	mA	Tristate Hi-Z (Output disabled)
	I _{DRV}	—	1.6	2	mA	0.8V LVCMOS (Load = 10pF // 10kΩ)
		—	2	2.5	mA	1.0V LVCMOS (Load = 10pF // 10kΩ)
		—	2.4	3	mA	1.2V LVCMOS (Load = 10pF // 10kΩ)
Frequency Range						
Frequency Range	F _{CLK}	10	—	76.8	MHz	Standard frequency options
		10, 16, 19.2, 20, 25, 26, 32, 38.4, 50, 52				Contact Aeonsemi for other frequency options
Frequency Tolerance						
Initial frequency accuracy ¹	F _{INIT}	-2	—	2	ppm	Grade C
		-5	—	5	ppm	Grade D
Temperature stability over full temp range ²	F _{STAB}	-0.5	—	0.5	ppm	Grade C
		-20	—	20	ppm	Grade D
Aging	S _{AGING}	-1	—	1	ppm/y	Maximum aging slope at 25 °C
	F _{AGING}	-3	—	3	ppm	10-year aging at 25 °C
<p>Notes:</p> <ol style="list-style-type: none"> 1. Inclusive of initial frequency tolerance at 25 °C, variations over supply voltage, load and humidity after 2 times of reflows. 2. Frequency / temperature characteristics with offset removed. 						
IO Characteristics						
Output enable (OE)	V _{IH}	0.7×V _{DD}	—	—	V	Input high voltage
	V _{IL}	—	—	0.3×V _{DD}	V	Input low voltage
	R _{PUP}	—	50	—	kΩ	Internal pull-up resistor to V _{DD}
	T _D	—	—	3	us	Output disable time, F _{CLK} > 10 MHz
	T _E	—	—	20	us	Output enable time, F _{CLK} > 10 MHz

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Characteristics						
Powerup time	T_{osc}	—	—	4	ms	Time from power reaches $0.9 \times V_{DD}$ to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	—	55	%	LVCMOS (Load = 10pF // 10kΩ)
Rise/Fall time (20% to 80% VPP)	$T_{R/F}$	—	0.5	1.5	ns	LVCMOS (Load = 10pF // 10kΩ)
LVCMOS	V_{OH}	$0.83 \times V_R$	—	—	V	Load = 10 pF // 10 kΩ
	V_{OL}	—	—	$0.17 \times V_R$	V	
Phase Noise and Jitter						
RMS jitter BW: 12k - 20MHz	R_J	—	100	200	fs	$F_{CLK} \geq 50$ MHz
		—	150	300	fs	$F_{CLK} < 50$ MHz
Phase noise 38.4MHz LVCMOS output $V_{DD} = 1.8 - 3.3$ V	PN ₁₀	—	-89	—	dBc/Hz	Phase noise at 10Hz offset
	PN ₁₀₀	—	-119	—	dBc/Hz	Phase noise at 100Hz offset
	PN _{1k}	—	-143	—	dBc/Hz	Phase noise at 1kHz offset
	PN _{10k}	—	-152	—	dBc/Hz	Phase noise at 10kHz offset
	PN _{100k}	—	-158	—	dBc/Hz	Phase noise at 100kHz offset
	PN _{1M}	—	-162	—	dBc/Hz	Phase noise at 1MHz offset
	PN _{10M}	—	-163	—	dBc/Hz	Phase noise at 10MHz offset
PSNR						
Spurs from power noise 50mV ripple $V_{DD} = 1.8$ V	PSNR	—	-76	—	dBc	100 kHz sine wave
		—	-75	—	dBc	200 kHz sine wave
		—	-75	—	dBc	500 kHz sine wave
		—	-75	—	dBc	1 MHz sine wave
Spurs from power noise 50mV ripple $V_{DD} = 2.5$ or 3.3 V	PSNR	—	-83	—	dBc	100 kHz sine wave
		—	-83	—	dBc	200 kHz sine wave
		—	-83	—	dBc	500 kHz sine wave
		—	-82	—	dBc	1 MHz sine wave

Table 2.2. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	3
Notes:	
For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us	

Table 2.3. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T _{AMAX}	125	°C
Storage temperature	T _S	-55 - 125	°C
Supply voltage	V _{DD,MAX}	-0.5 - 3.8	V
Input voltage	V _{IN,MAX}	-0.5 - V _{DD} +0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature ²	T _{PEAK}	260	°C
Solder time at T _{PEAK} ²	T _P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Package Outline Drawing

Figure 3.1. shows the package outline drawing for the AS5231 devices. Details of dimension for different size options are listed in Table 3.1.

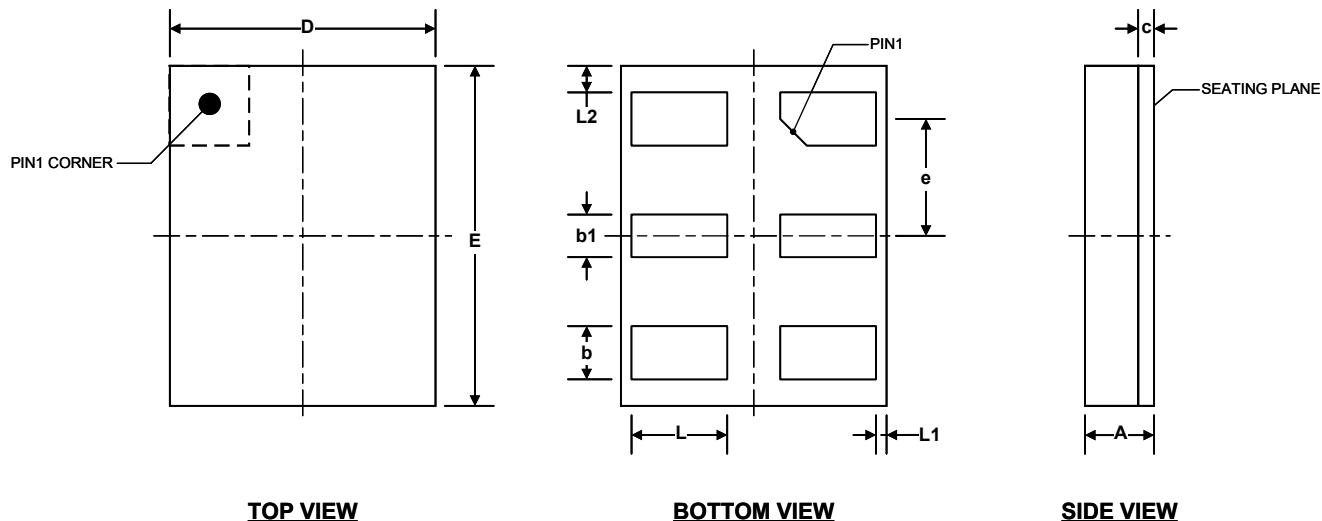


Figure 3.1. Package Outline Drawing

Table 3.1. Dimensions of Package Outline Drawing (mm)

Symbol	Min	Nom	Max
A	0.790	0.890	0.990
b	0.225	0.300	0.375
b1	0.225	0.300	0.375
D	1.550	1.600	1.650
e	—	0.750 BSC	—
E	1.950	2.000	2.050
L	0.375	0.450	0.525
L1	0.025	0.100	0.175

4. Recommended PCB Land Pattern

Figure 4.1. shows the drawing of recommended PCB land pattern for the AS5231 devices. Details of dimension for different size options are listed in Table 4.1.

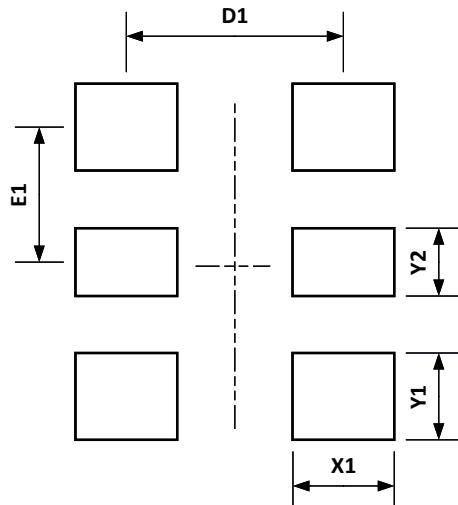


Figure 4.1. Recommended PCB Land Pattern

Table 4.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	2016 Package
D1	1.05
E1	0.75
X1	0.75
Y1	0.50
Y2	0.50

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. Top Mark

Figure 5.1. shows the top mark specifications for the AS5231 devices. Description of each line is listed in Table 5.1.

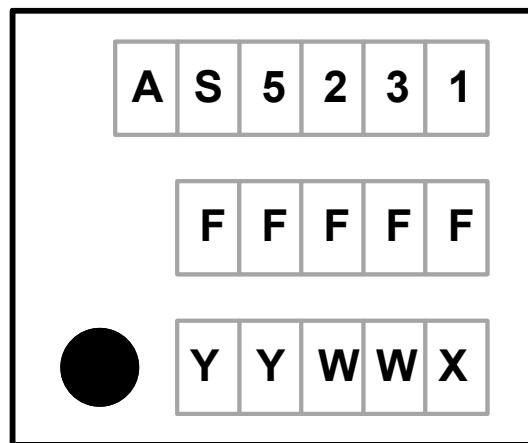


Figure 5.1. Top Mark

Table 5.1. Top Mark Description

Line	Position	Description
1	1-6	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

6. Important Notice and Disclaimer

Aeonsemi provides technical information such as datasheets, characterization reports, application notes, reference designs, and other resources "as is" and with all faults, and disclaims all warranties, express and implied, including without limitation any implied warranties of merchantability, fitness for a particular purpose or non-infringement of third-party intellectual property rights. These resources are subject to change without notice except when PCN is applicable. Aeonsemi grants you permission to use these resources only for development of an application that uses the Aeonsemi products described in the resource. Other reproduction and display of these resources are prohibited. No license is granted to any other Aeonsemi intellectual property right or to any third-party intellectual property right. Aeonsemi disclaims responsibility for, and you will fully indemnify Aeonsemi and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Aeonsemi's products are provided subject to Aeonsemi's Terms of Sale (aeonsemi.com/terms) or other applicable terms available either on aeonsemi.com or provided in conjunction with such Aeonsemi products.

Contact: marketing@aeonsemi.com

7. Revision History

Revision	Date	Description
1.02	Sep 2025	Corrected several description errors
1.01	Aug 2025	Officially release as mass production version
0.09	Feb 2025	Added “2016” package outline diagram
0.08	Aug 2024	Updated several items
0.07	Apr 2024	Remove the package outline drawings temporarily
0.06	Feb 2024	Updated the “Ordering guide”
0.05	Aug 2023	Revised the stability for D-grade option
0.04	Jul 2023	Updated the package outline
0.03	Jun 2023	Updated the “Ordering guide” and added phase noise jitter for clock ≥ 100 MHz
0.02	Feb 2023	Updated the “Temperature Stability Grade” D grade
0.01	Nov 2021	Preliminary release